SESSION DR1: Advances in Synthesis and Thermal Aware CAD
1:30 P.M.~2:50 P.M., Monday, April 27
Mezzanine A+B

Co-Chairs:
Yu-Min Lee, National Chiao Tung University, Taiwan
Chun Yao Wang, National Tsing Hua University, Taiwan

1:30 P.M.
DR11 ROBDD-Based Area Minimization Synthesis for Reconfigurable Single-Electron Transistor Arrays
Yi-Hang Chen, Yang Chen, and Juinn-Dar Huang
National Chiao Tung University, Taiwan

The power dissipation has become a crucial issue for most electronic circuit and system designs nowadays when fabrication processes exploit even deeper submicron technology. In particular, leakage power is becoming a dominant source of power consumption. In recent years, the reconfigurable single-electron transistor SET array has been proposed as an emerging circuit design style for continuing Moore’s Law due to its ultra-low power consumption. Several automated synthesis techniques for area minimization have been developed for the reconfigurable SET array in the past few years. Nevertheless, most of those existing methods focus on variable and product term reordering during SET mapping. In fact, minimizing the number of product terms can greatly reduce the area as well, which has not been well addressed before. In this paper, we propose a dynamic shifting based variable ordering algorithm that can minimize the number of disjoint sum-of-product terms extracted from the given ROBDD. Experimental results show that the proposed method can achieve an area reduction of up to 49H as compared to current state-of-the-art techniques.

1:50 P.M.
DR12 Dynamic Voltage Assignment for Thermal-Constrained Task Scheduler on 3D Multi-Core Processors
Chien-Hui Liao, Yu-Ze Lin, and Hung-Pin Wen
National Chiao Tung University, Taiwan

Thermal-constrained task scheduler for throughput optimization on 3D multi-core processors 3D-MCPs has been studied extensively. Most task scheduler focused on thermal-aware task allocation to reduce hotspots, thereby maximizing throughput under thermal constraints. Rather than focusing on the thermal-aware task allocation as previous work does, this work targets on the voltage assignment. In this paper, dynamic voltage assignment is proposed to pre-emptively assign different voltage levels to cores frequently for reducing temperature increase in 3D-MCPs. Experimental results show that two previous task schedulers integrated with the proposed dynamic voltage assignment can lower hotspot occurrences by 62.31H and 59.09H, and improve throughput by 18.28H and 18.35H, respectively. As a result, task schedulers integrated with the proposed dynamic voltage assignment can be more effective to reduce occurrences of hotspots and optimize throughput for 3D-MCPs under thermal constraints.

2:10 P.M.
DR13 An Effective Matrix Compression Method for GPU-Accelerated Thermal Analysis
Lih-Yih Chiou, Liang-Ying Lu, and Chieh-Yu Lin
National Cheng Kung University, Taiwan

Three-dimensional integrated circuits are expected to face increasingly severe thermal challenges and cost issues as the number of stacked ICs increases. Thermal analysis for 3D ICs is urgently required to assist system designers at the early phase of design to identify hot zones. Most thermal analyses obtain detailed temperature distribution by large matrix operations, and hence reduce analysis performance. Accordingly, we propose a compressed and combined sparse row (CCSR) matrix format to be used in the proposed effective matrix compression (EMC) method for matrix multiplication on GPU. The experimental results show EMC using CCSR is on average 44.93 times faster.
than matrix multiplication without any special compression format and on average at least 3.09 times faster than other compression formats.

2:30 P.M.
**DR14 Electro-Thermal Modeling of A Rogowski Coil Sensor System**
Juan Sebastian Rodriguez Estupinan¹, Alain Vachoux¹, and Joris Pascal²
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This paper focuses on the electro-thermal modeling of an electrical current sensor, based on the Rogowski Coil transducer. We exploit the multi-domain capabilities of VHDL-AMS together with geometrical Finite Element Analysis (FEA) to create a time-dependent parametrical model which is able to compute concurrently the thermal and electrical variables of the system. This is particularly convenient for evaluating the temperature effect in the analogue and digital signal processing of the sensor. Some key geometrical and inner material properties of the sensor and its environment, which are difficult, or even impossible to simulate dynamically in a classical lumped-element model, are taken into account in the proposed model. This modeling technique can be used to improve the accuracy in the design of the self-calibration circuit of the sensor.

2:50 P.M. ~ 3:10 P.M. Break